1. A method to form flash memory devices in the manufacture of an integrated circuit device comprising:

providing a substrate;

forming a first film comprising a first oxide layer overlying said substrate and a floating gate layer overlying said first oxide layer;

forming a second film comprising a second oxide layer overlying said first film, a control gate layer overlying said second oxide layer, and an insulating layer overlying said control gate layer;

patterning said first and second films to form stacked gates comprising floating gates and control gates;

implanting ions into said substrate between said stacked gates to form source and drain regions;

thereafter forming a third oxide layer on the sidewalls of said stacked gates;

thereafter depositing a plug layer overlying said substrate and said stacked gates and filling spaces between said stacked gates; and

etching down said plug layer to below the top surface of said stacked gates to form conductive plugs contacting said source and drain regions and to complete said flash memory devices.

2. The method according to Claim 1 wherein said floating gate layer comprises polysilicon.

3. The method according to Claim 1 wherein said control gate layer comprises polysilicon.

4. The method according to Claim 1 wherein said plug layer comprises polysilicon.

5. The method according to Claim 1 further comprising:

depositing a temporary film overlying said substrate prior to said step of forming said first film wherein said temporary film comprises a capping layer;

thereafter patterning said temporary film and said substrate to form trenches for STI regions that bound active areas where said flash devices are planned;

depositing a trench oxide overlying said temporary film and filling said trenches;

polishing down said trench oxide layer to below the top surface of said temporary film;

thereafter removing said capping layer wherein notches are formed at the top corners of said trench oxide adjacent to said temporary film;

thereafter removing remaining said temporary film such that said trench oxide of said STI regions protrudes substantially above said substrate; and

etching down said floating gate layer prior to said step of forming said second film wherein said floating gate layer remains only in areas between said STI regions and wherein the surface profile of said floating gate layer is angled to enhance an electric field.

6. The method according to Claim 5 further comprising etching said trench oxide after said step of etching down said floating gate layer to thereby expose tips of said floating gate layer.

7. The method according to Claim 1 further comprising:

forming a masking layer overlying said plug layer coupled to said sources;

depositing a bit line layer overlying said plug layer said masking layer, and said stacked gates;

patterning said bit line layer and exposed said plug layer to form bit lines and to form source lines.

8. A method to form flash memory devices in the manufacture of an integrated circuit device comprising:

providing a substrate;

depositing a temporary film overlying said substrate prior to said step of forming said first film wherein said temporary film comprises a capping layer;

patterning said temporary film and said substrate to form trenches for STI regions that bound active areas where said flash devices are planned;

depositing a trench oxide overlying said temporary film and filling said trenches;

polishing down said trench oxide layer to below the top surface of said temporary film;

thereafter removing said capping layer wherein notches are formed at the top corners of said trench oxide adjacent to said temporary film;

thereafter removing remaining said temporary film such that said trench oxide of said STI regions protrudes substantially above said substrate;

forming a first film comprising a first oxide layer overlying said substrate and a floating gate layer overlying said first oxide layer;

etching down said floating gate layer wherein said floating gate layer remains only in areas between said STI regions and wherein the surface profile of said floating gate layer is angled to enhance an electric field;

thereafter forming a second film comprising a second oxide layer overlying said first film, a control gate layer overlying said second oxide layer, and an insulating layer overlying said control gate layer;

patterning said first and second films to form stacked gates comprising floating gates and control gates;

implanting ions into said substrate between said stacked gates to form source and drain regions;

thereafter forming a third oxide layer on the sidewalls of said stacked gates;

thereafter depositing a plug layer overlying said substrate and said stacked gates and filling spaces between said stacked gates; and

etching down said plug layer to below the top surface of said stacked gates to form conductive plugs contacting said source and drain regions and to complete said flash memory devices.

9. The method according to Claim 8 wherein said floating gate layer comprises polysilicon.

10. The method according to Claim 8 wherein said control gate layer comprises polysilicon.

11. The method according to Claim 8 wherein said plug layer comprises polysilicon.

12. The method according to Claim 8 further comprising etching said trench oxide after said step of etching down said floating gate layer to thereby expose tips of said floating gate layer.

13. The method according to Claim 8 further comprising:

forming a masking layer overlying said plug layer coupled to said sources;

depositing a bit line layer overlying said plug layer said masking layer, and said stacked gates; and

patterning said bit line layer and exposed said plug layer to form bit lines and to form source lines.

14. A flash memory device comprising:

a substrate;

a stacked gate comprising a floating gate and a control gate wherein said floating gate comprises a first oxide layer overlying said substrate and a floating gate layer overlying said first oxide layer and wherein said control gate comprises a second oxide layer overlying said floating gate layer and a control gate layer overlying said second oxide layer;

source and drain regions in said substrate adjacent to said stacked gate;

a third oxide layer on the sidewalls of said stacked gate; and

a conductive plugs contacting said source and drain regions wherein said conductive plugs extend parallel to said stacked gate and wherein said conductive plug layer provides coupling of between said drain and source and said floating gate.

15. The device according to Claim 14 wherein said floating gate layer comprises polysilicon.

16. The device according to Claim 14 wherein said control gate layer comprises polysilicon.

17. The device according to Claim 14 wherein said conductive plugs comprises polysilicon.

18. The device according to Claim 14 wherein the surface profile of said floating gate layer is angled to enhance an electric field.

19. The device according to Claim 14 wherein adjacent stacked gates are separated by STI regions that protrude substantially above said substrate.

20. The device according to Claim 14 further comprising:

a masking layer overlying said conductive plug coupled to said source;

a patterned bit line layer overlying said conductive plug coupled to said drain, said masking layer, and said stacked gates.

21. The device according to Claim 20 wherein said patterned bit line layer comprises polysilicon.

22. The device according to Claim 14 wherein said floating gate is programmed by forcing a negative voltage across said control gate and said source and drain conductive plugs.

23. The device according to Claim 14 wherein said floating gate is erased by forcing a positive voltage across said control gate and said source and drain conductive plugs.

24. The device according to Claim 14 wherein said floating gate is erased by forcing a first positive voltage across said control gate and said source conductive plug and a second, smaller positive voltage across said control gate and said drain conductive plug.

25. The device according to Claim 14 wherein said floating gate is read by forcing a first positive voltage across said control gate and said source conductive plug and a second, smaller positive voltage across said control gate and said drain conductive plug.